WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a programmable logic portion;

a first JTAG circuit, wherein the first JTAG circuit comprises a first TAP controller coupled to a first instruction register and a first plurality of data registers; and

an embedded logic portion comprising a processor and a second JTAG circuit coupled to the first JTAG circuit and to the processor, wherein the second JTAG circuit comprises a second TAP controller coupled to a second instruction register and a second plurality of data registers.

2. The integrated circuit of claim 1 wherein one of the first plurality of data registers comprises a data register that is used to load data into the programmable logic portion to configure logic circuitry in the programmable logic portion.

3. The integrated circuit of claim 1 wherein one of the first plurality of data registers comprises a data register that is allows a user to transmit and receive data from the programmable logic portion.

4. The integrated circuit of claim 1 wherein one of the second plurality of data registers comprises a first data register that acts as a communications interface between the embedded logic portion of the integrated circuit and an external host processor.

5. The integrated circuit of claim 4 wherein the external host processor loads first action bits into the first data register indicating a first action to be performed by circuitry in the embedded logic portion, and wherein second action bits may not be loaded into the first data register until the first action has been performed and the first data register has communicated results of the first action to the external host processor.

6. The integrated circuit of claim 4 wherein the external host processor selects a variable length scan chain as the first data register.

7. The integrated circuit of claim 6 wherein the variable length scan chain is synchronized between the external host processor and the processor in the embedded logic portion using a particular pattern of ones and zeros.

8. The integrated circuit of claim 7 wherein the particular pattern of ones and zeros is one bit long and has a value of one.

9. The integrated circuit of claim 1 wherein the second plurality of data registers are coupled to a first multiplexer that is controlled by data signals decoded from the second instruction register.

10. The integrated circuit of claim 9 wherein an output of the first multiplexer, the second instruction register, and a test data output of the first JTAG circuit are coupled to a second multiplexer that is controlled by the second TAP controller.

11. An embedded logic portion of an integrated circuit, the integrated circuit comprising a programmable logic portion, the embedded logic portion comprising:

a processor; and

a first JTAG circuit coupled to the processor and a second JTAG circuit that is part of control logic for the programmable logic portion, wherein the first JTAG circuit comprises a first TAP controller that outputs a plurality of control signals that control a first instruction register and a first plurality of data registers.

12. The embedded logic portion of claim 11 wherein the second JTAG circuit comprises a second plurality of data registers coupled to a second TAP controller, and wherein one of the second plurality of data registers comprises a bypass register that does not perform any function.

13. The embedded logic portion of claim 11 wherein the second JTAG circuit comprises a second plurality of data registers coupled to a second TAP controller, and wherein one of the second plurality of data registers comprises a data register that can force data onto and capture data from a plurality of input/output pins.

14. The embedded logic portion of claim 11 wherein the second JTAG circuit comprises a second plurality of data registers coupled to a second TAP controller, and wherein one of the second plurality of data registers comprises a data register that is used to load data into the programmable logic portion to configure logic circuitry in the programmable logic portion.

15. The embedded logic portion of claim 11 wherein the second JTAG circuit comprises a second plurality of data registers coupled to a second TAP controller, and wherein one of the second plurality of data registers comprises a data register that allows a user to transmit and receive data from the programmable logic portion on input/output pins.

16. The embedded logic portion of claim 11 wherein one of the first plurality of data registers comprises a first data register that acts as a communications interface between the embedded logic portion and an external host processor.

17. The embedded logic portion of claim 16 wherein the external host processor loads first action bits into the first data register indicating a first action to be performed by circuitry in the embedded logic portion, and wherein second action bits may not be loaded into the first data register until the first action has been performed and the first data register has communicated results of the first action to the external host processor.

18. The embedded logic portion of claim 16 wherein the external host processor selects a variable length scan chain as the first data register.

19. The embedded logic portion of claim 11 wherein the first plurality of data registers are coupled to a first multiplexer that is controlled by data signals decoded from the first instruction register.

20. The embedded logic portion of claim 19 wherein an output of the first multiplexer, the first instruction register, and a test data output of the second JTAG circuit are coupled to a second multiplexer that is controlled by the first TAP controller.

21. A method for testing data using a chip that comprises a first processor and a programmable logic portion, comprising:

transmitting first data signals between pins and circuitry in the programmable logic portion using a first JTAG circuit; and

transmitting second data signals between an external host processor and the first processor using a second JTAG circuit in an embedded logic portion of the chip.

22. The method of claim 21 wherein the first and second JTAG circuits comprise first and second TAP controllers, respectively.

23. The method of claim 21 wherein transmitting the first data signals further comprises loading the first data signals into the programmable logic portion to configure logic circuitry in the programmable logic portion using a data register that is part of the first JTAG circuit. circuit.

24. The method of claim 21 wherein transmitting the second data signals further comprises transmitting the second data signals between the external host processor and the embedded logic portion using a data register that is part of the second JTAG circuit.

25. The method of claim 21 transmitting the second data signals further comprises selecting from a plurality of data registers in the second JTAG circuit using a first multiplexer that is controlled by signals decoded from an instruction register.

26. The method of claim 25 wherein transmitting the second data signals further comprises selecting from an output of the first multiplexer, an output of the instruction register, and a test data output of the first JTAG circuit using a second multiplexer that is controlled by a TAP controller in the second JTAG circuit.

27. An integrated circuit, comprising:

a processor comprising a first JTAG circuit, wherein the first JTAG circuit comprises a first TAP controller coupled to a first instruction register and a first plurality of data registers; and

a second JTAG circuit coupled to the first JTAG circuit, wherein the second JTAG circuit comprises a second TAP controller coupled to a second instruction register and a second plurality of data registers.

28. The integrated circuit of claim 27 wherein the integrated circuit comprises an embedded logic portion and a programmable logic portion, and wherein the second JTAG circuit is part of an embedded logic portion of the integrated circuit.

29. The integrated circuit of claim 28 wherein the second JTAG circuit comprises a multiplexer having a first input coupled to an output of the first JTAG circuit and a second input coupled to receive data signals from one of the second plurality of data registers.